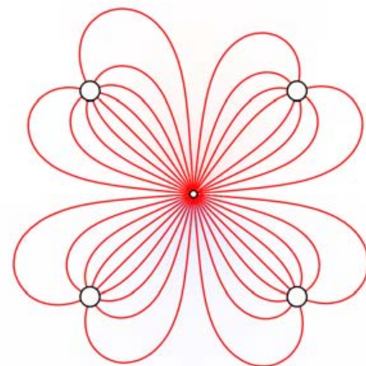
Electroplating & Lithography as Techniques to mass-produce Micro-Targets



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Sequential & Parallel Target Production

Lithography:

sequentially written
(structured) mask

Information / structure

→

Imaging: Photons

Electroplating:

sequentially manufactured
structured electrode

Information / structure

→

E-field: Ions

Individual process steps
applied to a great numbe
of targets in parallel

Individual process steps
applied to a great numbe
of targets in parallel

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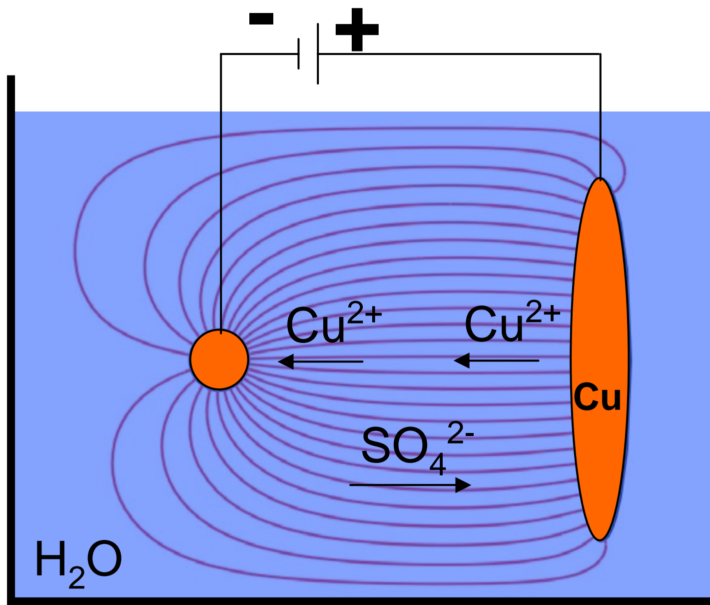
Electroforming / Plating



- Individual ions move along E-field lines
- Local growth rate ~ to E-field strength
- Either anode or cathode can be the sample to be shaped

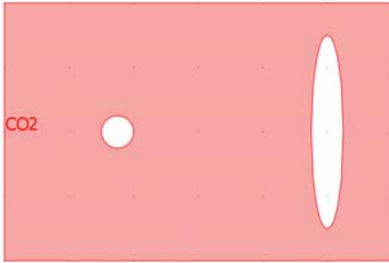
Homogeneous 2D-layer: Smooth E-field configuration

Inhomogeneous deposition: 3D-structure

- Specifically shaped electrode
- Small distance between electrode and substrate

How to predict the surface shape change?

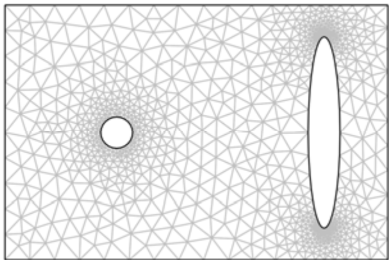
Simulating the Plating Process: Comsol



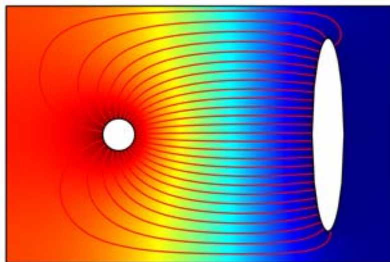
- Define the geometry (CAD import)
- Set domain & boundary conditions:
  electrolyte conductivity / source current, etc.
- Define boundary growth rate: $G_m = K \times J_n = 2.88 \frac{\mathrm{nm}}{s}$

$$K[\mathrm{m}^3/\mathrm{C}] = \frac{10^{-6}}{\rho[\mathrm{g/cm}^3]} \frac{A_r[\mathrm{g/mol}]}{N_A[1/\mathrm{mol}]} \frac{1}{Z\,e[\mathrm{C}]}$$

$$J_n[\mathrm{C\ /s\ m}^2] = 30\ \frac{\mathrm{A}}{\mathrm{m}^2}$$



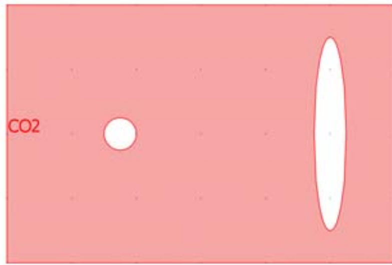
- Meshing for the finite element solver

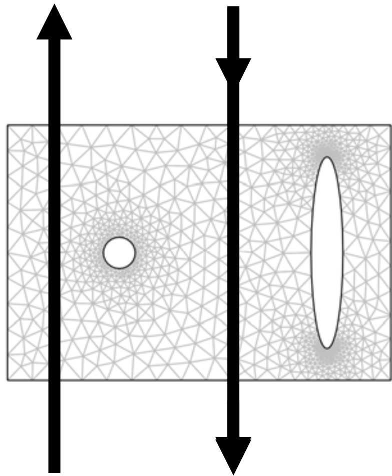


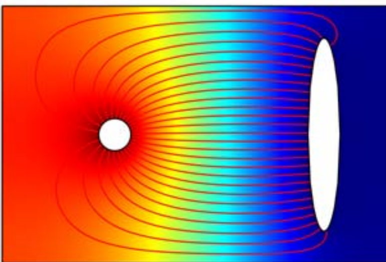
- Solve for the electric field / current density distribution:

$$-\nabla \cdot (\sigma \nabla V - \vec{J}) = Q_j$$

Simulating the Plating Process: Comsol



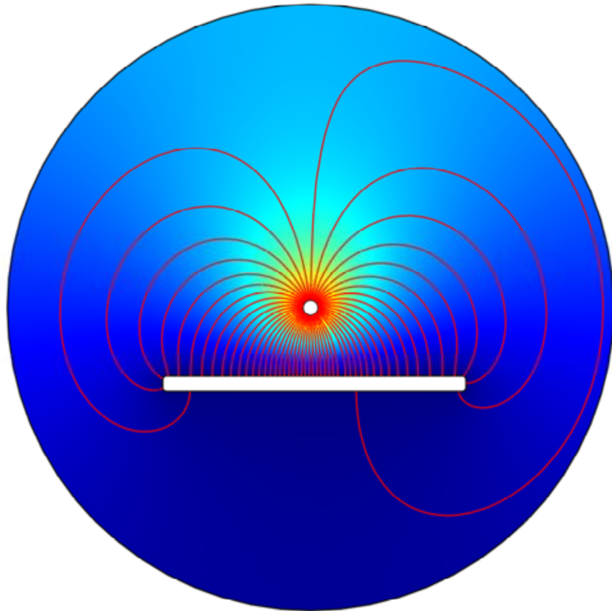


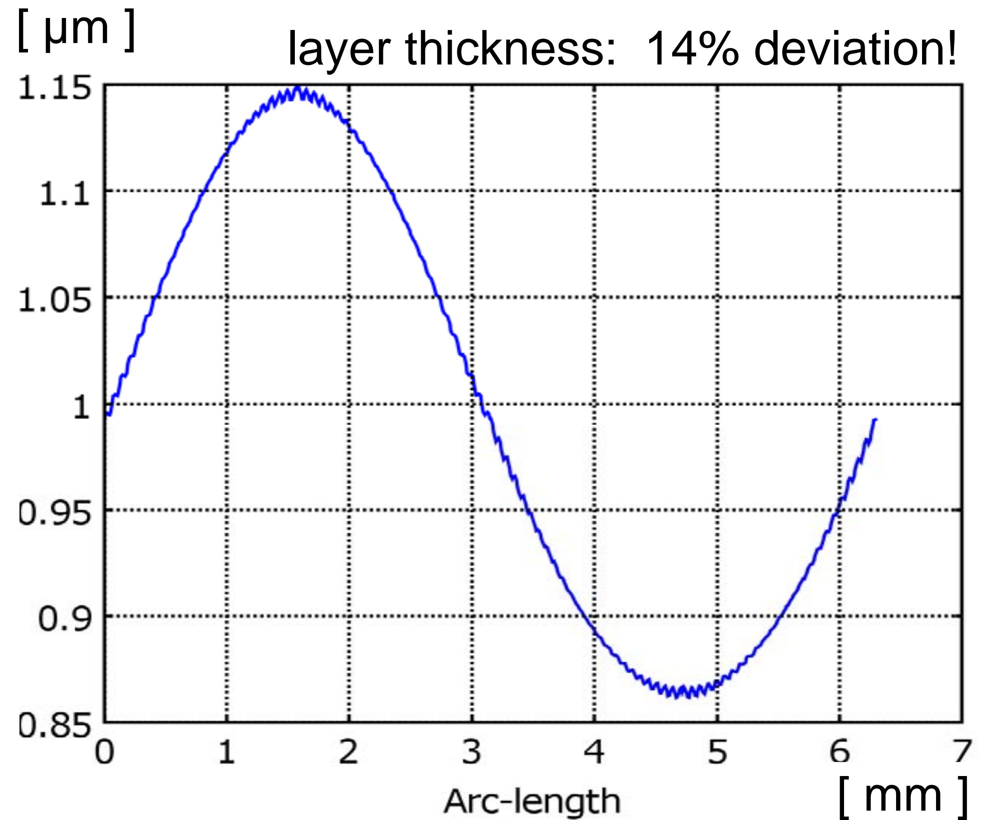


- Iterative process:
  - Geometry changes at each time step
  - E-field & local current density changes

- Deformable mesh
- Monitor the mesh quality:
  - remesh, if necessary

Calculation: R=1mm rod / distance 1cm





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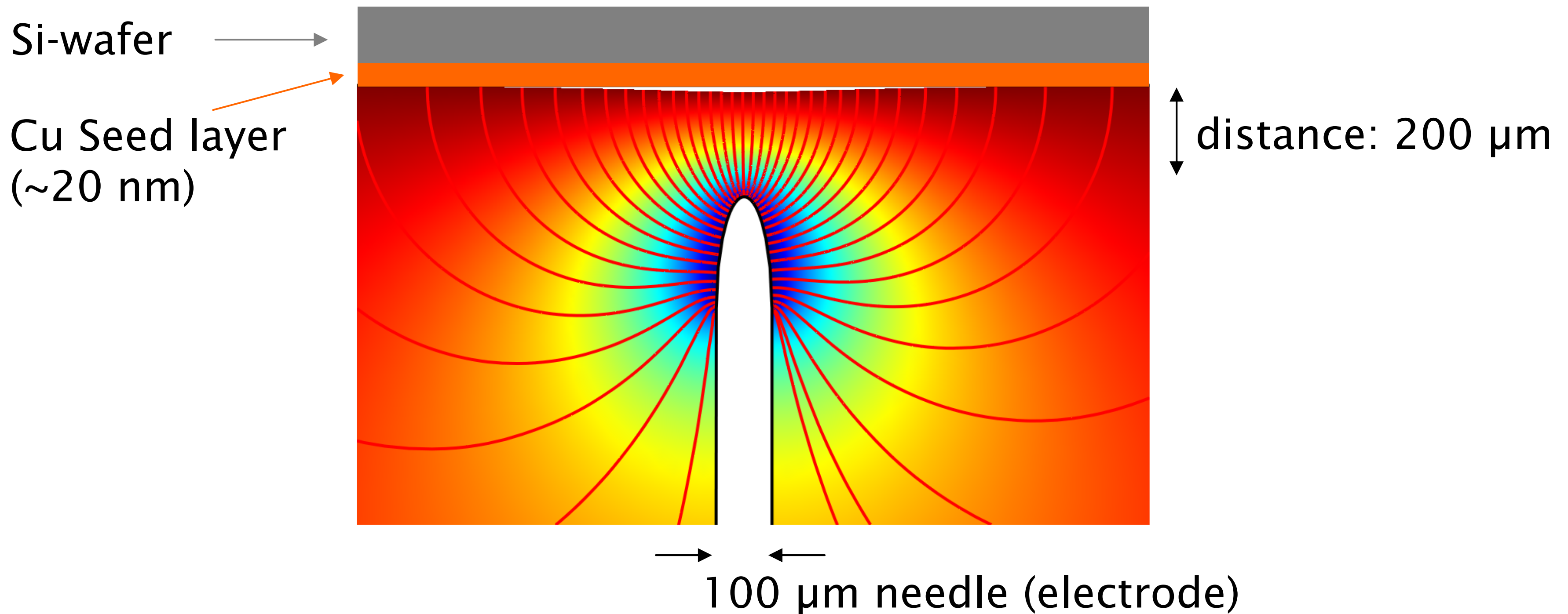
Calculation: Dimple on a foil target



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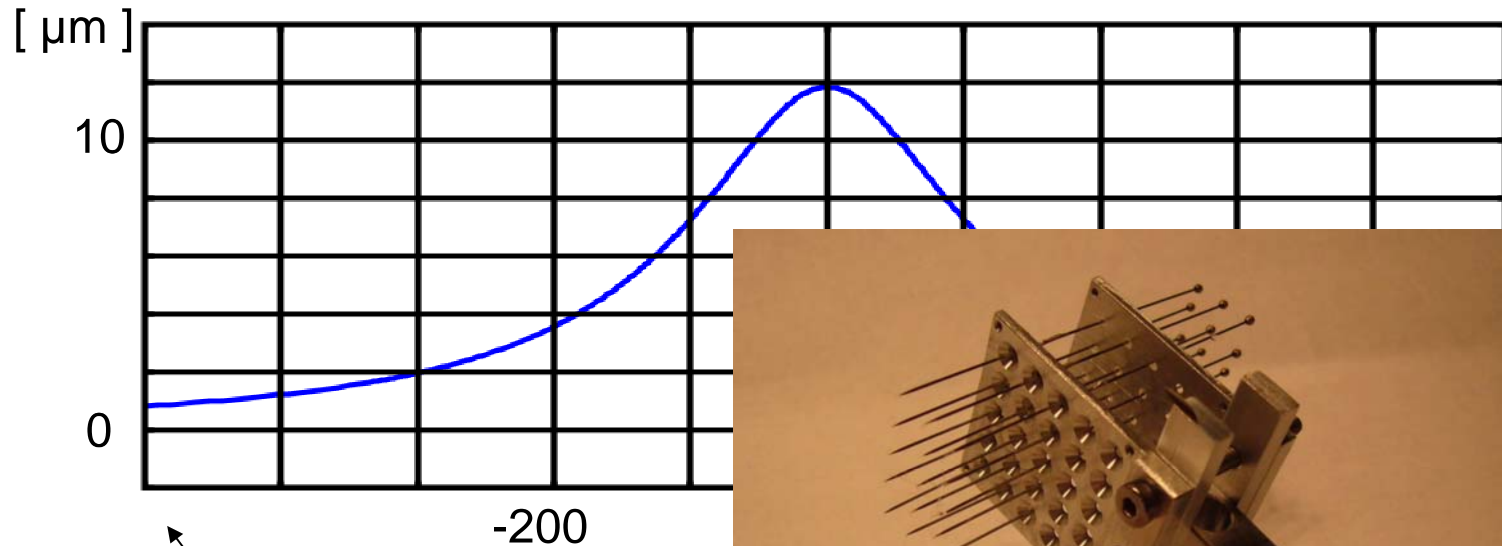
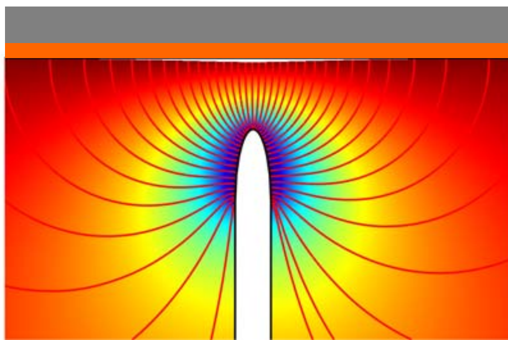
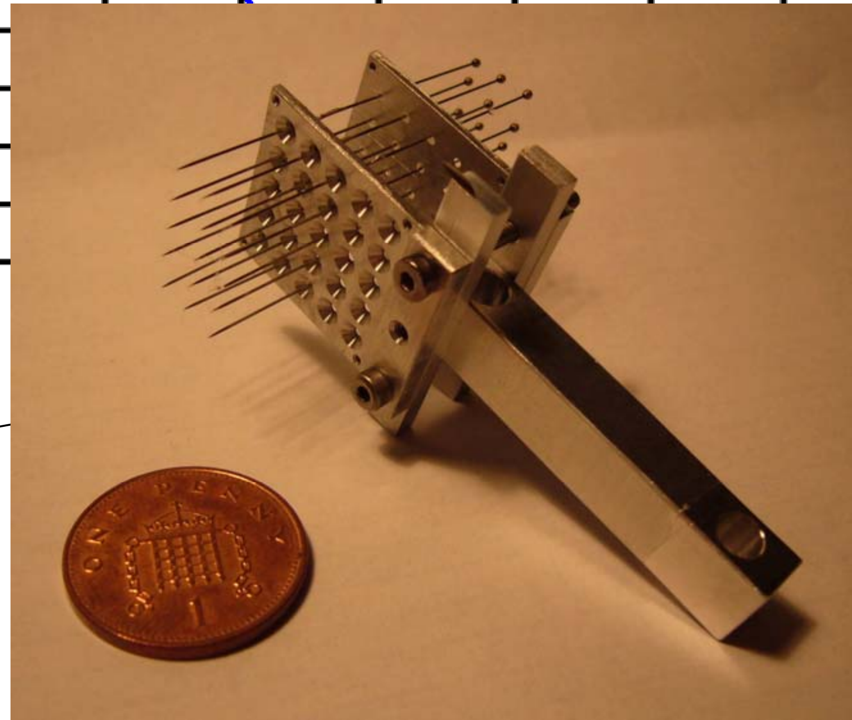
Calculation: Dimple on a foil target







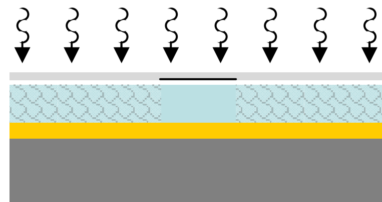
Electroplating & Lithography

Requirement & Opportunity for plating: Substrate needs to be conductive!

- Protective layer of non conductive material: Photo resist.
- Photo resist can be structured: Photo lithography
- Plate 3D structures with high aspect ratio

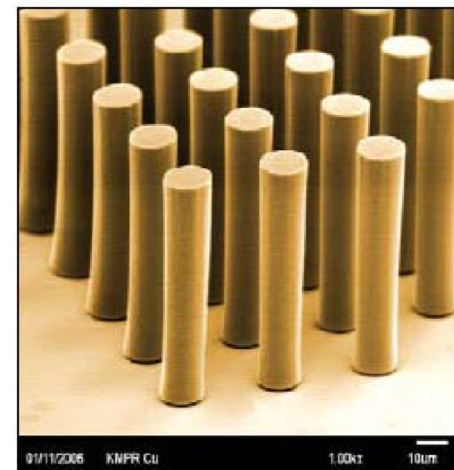
Simple example process:

Mask & exposure
Resist
Au seed layer
Si-wafer



Develop
&
Plate

Remove resist



50 µm tall Cu pins
@ micro-chem.com

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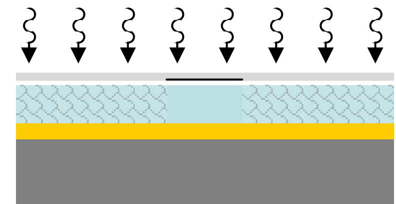
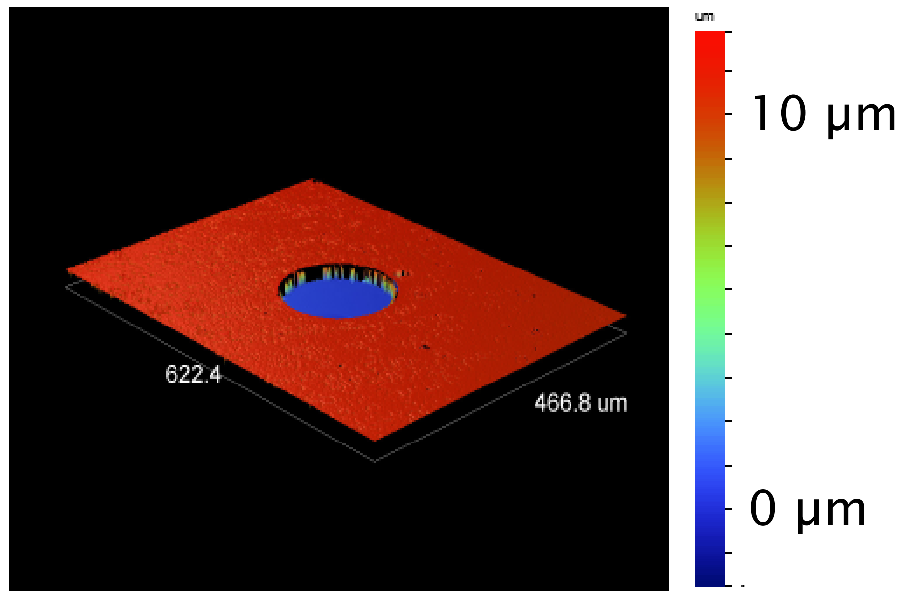
First experimental tests at TFG

- 3'' Si-wafer
- Sputtered with 20nm Cr layer (adhesion)
- Sputtered with 50nm Au seed layer
- Spin-coated with 10µm photo resist (SU8)
- Exposed with UV-light / dot mask / developed





150 µm Dot

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Touch probe: Section profile

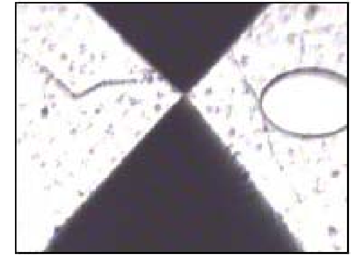
Resist: 10µm

µm

2
0
-2
-4
-6
-8
-10
-12
-14
-16

L
R

0 100 200 300 400 500 600 700 800 900 1000 µm



Alpha-Step IQ

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Touch probe: Section profile

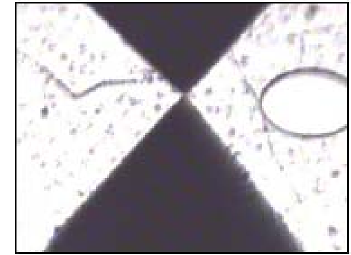
Plated: 2µm

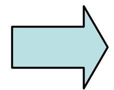
µm

0
-1
-2
-3
-4
-5
-6
-7
-8
-9

L
R

0 100 200 300 400 500 600 700 800 900 1000 µm





Alpha-Step IQ

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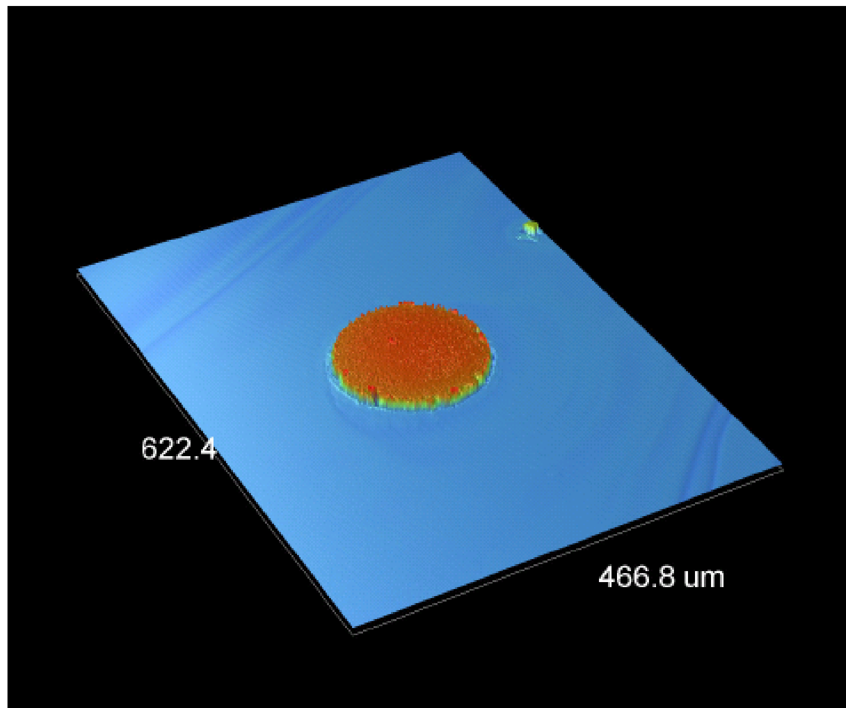
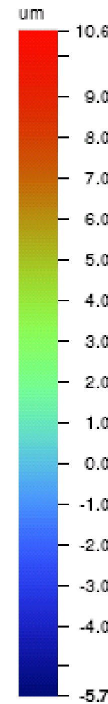
Gold plated Pins on a Wafer Substrate

3-Dimensional Interactive Display

Date: 10/23/2008
Time: 12:53:12





150 μm dot
8 μm height on Au foil

Thanks

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- Martin Tolley

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